Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A method comprising;

placing one or more signal lines substantially between a match line and a data line in a CAM memory cell.

2. (original) The method of claim 1 further comprising placing a second set of one or more signal lines substantially between said match line and a substantially inverted version of said data line in said CAM memory cell.

3. (original) The method of claim 2 wherein said one or more signal lines and said second set of one or more signal lines are not the same signal lines.

4. (original) The method of claim 2 wherein said one or more signal lines and said second set of one or more signal lines are selected from the group consisting of a positive voltage supply, a ground signal, a value bit, a data bit, a mask bit, a substantially inverted version of said value bit, a substantially inverted version of said data bit, and a substantially inverted version of said mask bit.

5. (original) The method of claim 4 wherein said match line is selected from the group consisting of a low match line, and a high match line.

Claims 6-7 (canceled)

8. (original) A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

coupling any remaining said less than all memory cells to a second sense amplifier and;

routing a data line substantially parallel to a match line, but not directly adjacent to said match line.

9. (original) A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a first input of a multiple input sense amplifier;

coupling any remaining said less than all memory cells to one or more inputs other than said first input of said sense amplifier;

routing one or more signal lines between a low match line and a data line; and

routing one or more signal lines between said low match line and a complement of said data line.

10. (original) The method of claim 9 wherein said multiple input sense amplifier is a two input sense amplifier.

11. (original) The method of claim 10 wherein said one or more signal lines is selected from the group consisting of a voltage supply, a ground signal, a value bit, a data bit, a mask bit, a complement of said value bit, a complement of said data bit, and a complement of said mask bit.

12. (original) A method for connecting cells in a row in a CAM sub-array, the method comprising:

separating a row match line into several submatch lines;

coupling less than all said cells in said row to a same sense amplifier; and

placing a trace between a low match line and a data line.

13. (original) The method of claim 12 further comprising:

coupling any remaining said less than all said cells to one or more sense amplifiers; and

placing a trace between said low match line and a complement of said data line.

14. (original) The method of claim 13 wherein said placing a trace is achieved using a substantially same set of interconnect layers.

15. (original) The method of claim 13 wherein said placing a trace is achieved using a substantially different set of interconnect layers.

16. (original) The method of claim 12 wherein said low match line and said data line are substantially parallel in routing.

17. (original) A method for constructing an integrated circuit (IC) content addressable memory (CAM) comprising:

connecting less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

connecting any remaining said less than all memory cells in said row of said sub-array of said CAM to a second sense amplifier; and

routing one or more signal lines between a match line and a compare data line and a complement of said compare data line associated with said memory cells in said row of said sub-array of said CAM.

18. (original) The method of claim 17 wherein said connecting and routing uses a substantially different set of interconnect layers.

Claim 19 (canceled)

20. (previously presented) An apparatus comprising:

a plurality of memory cells arranged in a row;

one or more match lines running substantially parallel to said row;

means for connecting two or more subsets of said plurality of memory cells to said one or more match lines; and

one or more low match lines running substantially perpendicular to said row;

one or more traces interspersed between said one or more low match lines and one or more data lines running substantially parallel to said one or more low match lines.

21. (original) The apparatus of claim 20 wherein said plurality is a sub-array.

22. (original) The apparatus of claim 20 wherein said one or more match lines connect to one or more sense amplifiers.

23. (original) The apparatus of claim 20 wherein said one or more match lines connect to one or more inputs of a sense amplifier.

24. (original) The apparatus of claim 20 wherein said means for connecting uses a substantially same set of integrated circuit interconnect layers.

25. (original) The apparatus of claim 20 wherein said means for connecting uses a substantially different set of integrated circuit interconnect layers.

26. (original) The apparatus of claim 20 wherein said means for connecting uses a same integrated circuit interconnect layer for a majority of distance of said one or more match lines.

27. (original) The apparatus of claim 20 wherein said means for connecting uses a different integrated circuit interconnect layer for a majority of distance of said one or more match lines.

28. (original) An apparatus comprising:

means for connecting memory cells in a row to two or more high match lines; and

means for routing a trace between a low match line and a data line.

29. (original) The apparatus of claim 28 wherein less than all of said memory cells in said row are connected to a first high match line.

30. (original) The apparatus of claim 29 wherein remaining less than all of said memory cells in said row are connected to one or more high match lines.

31. (original) The apparatus of claim 30 further comprising:

an integrated circuit containing said memory cells in a row; and

said connection to said first high match line is through a substantially same set of integrated circuit interconnect layers as said connection to said one or more high match lines.

32. (original) The apparatus of claim 31 further comprising said first high match line connected to a first amplifier and said one or more high match lines connected to one or more amplifiers.

33. (original) The apparatus of claim 31 further comprising said first high match line connected to a first input of an N input amplifier and each said one or more high match lines connected to one or more inputs of said N input amplifier.

34. (original) The apparatus of claim 32 wherein said connection to said first amplifier is through a substantially same set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

35. (original) The apparatus of claim 32 wherein said connection to said first amplifier is through a substantially different set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

36. (original) The apparatus of claim 30 further comprising:

an integrated circuit containing said memory cells in a row; and

said connection to said first high match line is through a substantially different set of integrated circuit interconnect layers as said connection to said one or more high match lines.

37. (original) The apparatus of claim 36 further comprising said first high match line connected to a first amplifier and said one or more high match lines connected to one or more amplifiers.

38. (original) The apparatus of claim 37 wherein said connection to said first amplifier is through a substantially same set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

39. (original) The apparatus of claim 37 wherein said connection to said first amplifier is through a substantially different set of integrated circuit interconnect layers as said connection to said one or more amplifiers.

40. (original) A CAM comprising:

cells arranged in a row wherein less than all of said cells in said row are in communication with a single submatch line;

a first match line substantially parallel with said row and in communication with one or more said cells; and

a second match line in communication with one or more said cells.

41. (original) The CAM of claim 40 further comprising one or more submatch lines in communication with any remaining cells not in communication with said single submatch line.

42. (original) The CAM of claim 41 wherein a particular cell is in communication with a submatch line selected from the group consisting of said single submatch line, said one or more submatch lines, and any combination of said single submatch line and said one or more submatch lines.

43. (original) The CAM of claim 41 further comprising a single sense amplifier coupled to receive input from said one or more submatch lines and said single submatch line.

44. (original) The CAM of claim 41 further comprising a plurality of sense amplifiers coupled to receive input from a source selected from the group consisting of said one or more submatch lines, said single submatch line, and any combination of said one or more submatch lines and said single submatch line.

45. (original) The CAM of claim 41 wherein said submatch lines are substantially of a same length.

46. (original) The CAM of claim 41 wherein said submatch lines are of different lengths.

47. (original) The CAM of claim 41 wherein said submatch lines use substantially the same IC interconnect layers.

48. (original) The CAM of claim 41 wherein said submatch lines use different IC interconnect layers.

49. (original) The CAM of claim 41 wherein said submatch lines are substantially of a same capacitance.

50. (original) The CAM of claim 41 wherein a particular cell is in communication with said one or more submatch lines and said single submatch line.

51. (original) A machine-readable medium having stored thereon information representing the apparatus of claim 40.

Claims 52-61 (canceled)

62. (original) A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

coupling any remaining said less than all memory cells to a second sense amplifier and;

routing one or more lines between a data line and a match line via.

63. (original) A method comprising:

coupling less than all memory cells in a row of a sub-array of a CAM to a first input of a multiple input sense amplifier;

coupling any remaining said less than all memory cells to one or more inputs other than said first input of said sense amplifier;

routing one or more lines between a low match line pickup via and a data line; and

routing one or more lines between said low match line and a complement of said data line.

64. (original) The method of claim 63 wherein said multiple input sense amplifier is a two input sense amplifier.

65. (original) The method of claim 64 wherein said one or more lines is selected from the group consisting of a voltage supply, a ground signal, a value bit, a data bit, a mask bit, a complement of said value bit, a complement of said data bit, and a complement of said mask bit.

66. (original) A method for connecting cells in a row in a CAM sub-array, the method comprising:

separating a row match line into several submatch lines;

coupling less than all said cells in said row to a same sense amplifier; and

placing a trace between a match line pickup via and a data line.

67. (original) A method for constructing an integrated circuit (IC) content addressable memory (CAM) comprising:

connecting less than all memory cells in a row of a sub-array of a CAM to a same sense amplifier;

connecting any remaining said less than all memory cells in said row of said sub-array of said CAM to a second sense amplifier; and

routing one or more signal lines between a match line pickup via and a compare data line and a complement of said compare data line associated with said memory cells in said row of said sub-array of said CAM.

68. (original) An apparatus comprising:

a plurality of memory cells arranged in a row;

one or more match lines running substantially parallel to said row;

vias for connecting one or more said memory cells to said one or more match lines; and

one or more traces between said vias and data lines.

Claims 69-84 (canceled)

85. (original) A method for connecting cells in a row in a CAM sub-array, the method comprising:

separating a row match line into several submatch lines;

coupling less than all said cells in said row to a same sense amplifier; and

placing a trace between a data line pickup via and a match line.

86. (original) An apparatus comprising:

a plurality of memory cells arranged in a row;

one or more data lines running substantially perpendicular to said row;

vias for connecting one or more said memory cells to said one or more data lines; and

one or more traces between said vias and match lines.

Claim 87 (canceled)